

Biwei Xie | Curriculum Vitae

Center for Advanced Computer Systems, ICT.CAS.
NO. 6, Kexueyuan South Road, Zhongguancun,
Haidian district, Beijing, P.R.China 100190.

📞 +86 13269199831 • ✉ xiebiwei@ict.ac.cn • 🌐 puckbee.github.io

Education

- **The Institute of Computing Technology, Chinese Academy of Sciences** **Beijing**
Ph.d. in Computer Science, Advisor: Prof. Lixin Zhang and Prof. Jianfeng Zhan **2012–2018**
Dissertation: Optimization of Data Analytics Workloads on Many-core Architecture
- **The Beijing University of Technology** **Beijing**
M.S. in Software Engineer, Advisor: Prof. Jingsha He **2009–2012**
Dissertation: Research on Distributed Intrusion Detection in Wireless Sensor Networks
- **Hebei University of Science and Technology** **ShiJiaZhuang**
B.S. in Software Engineer, **2005–2009**

Research Interest

Benchmarking, Performance Optimization, Operating System, and Computer Architecture.

Professional Experience

- **Institute of Computing Technology, Chinese Academy of Sciences** **Beijing**
Assistant Professor **July 2018 – Now**
I am working with Prof. Yungang Bao on some projects related to high performance computing and computer architecture. Besides, I'm now getting familiar with Verilog and Chisel. My work will focus on computer architecture design in the following several years.

Ongoing Projects

- **HPCConv (2017 ~ Now):** *High performance winograd-based convolution*
This project aims at a high performance implementation of winograd-based convolution, considering sparse, cross-layer data fusion, and strassen based matrix multiplication(MM). HPCConv is preliminary designed for inference-convolution and will be extended to training-convolution in the future.
- **SparseLib(2017 ~ Now):** *High performance library for sparse problems*
Numerous applications rely on sparse linear algebra methods or can be reduced to sparse problems. SparseLib focuses on exploiting architectural advances on emerging hardware (wider SIMD lanes on Xeon Phi; massive processing units on GPU;...) for various sparse related operations, like SpMV, SpMM, sparseFFT, and etc.

Previous Projects

- **PhiBench(2014 ~ 2016):** *Understanding data analytics workloads on x86 based many-core processors*
The first release of PhiBench consists of eight data analytics workloads, which are delicately optimized on Intel Xeon Phi, an x86 based many-core processor. We hope that PhiBench is useful for researchers that are interested in understanding data analytics workloads on Intel Xeon Phi.
- **mobile-Tracking(2014 ~ 2015):** *Optimizing body-tracking algorithms on mobile platform*
In this project, we optimize a HOG+FFT based tracking algorithm on NVIDIA TK1. The raw code is written in C/Matlab. We need to investigate the hotspot and accelerate it through parallelization and vectorization.
- **xMem(2013 ~ 2015):** *Enlarging the memory on co-processors with host memory*
Memory capacity on many co-processors is limited, and unlike host memory, it's hard to increase. In this project, rarely used data on co-processors will be swapped to host memory. Different from classical swap mechanism, swap partition in this project is writable, and can be used for communication between host and co-processors.
- **pQEMU(2012 ~ 2013):** *Parallel version of QEMU*
QEMU is serial, even when it emulates multiple processors and runs on a multi-core processor. pQEMU aims at accelerating QEMU through multi-threading.

Publications

- **[PACT'18] Data Motifs: A Lens Towards Fully Understanding Big Data and AI Workloads.** Wanling Gao, Jianfeng Zhan, Lei Wang, Chunjie Luo, Daoyi Zheng, Fei Tang, **Biwei Xie**, Chen Zheng, Xu Wen, Xiwen He, Hainan Ye, and Rui Ren. In Proceedings of the 27th International Conference on Parallel Architectures and Compilation Techniques. To Appear. Nov 01-04, 2018, Limassol, Cyprus.
- **[ICS'18] Towards efficient SpMV on sunway many-core architectures.** Changxi Liu, **Biwei Xie**, Xin Liu, Wei Xue, Hailong Yang, and Xu Liu. In Proceedings of the 2018 International Conference on Supercomputing. Jun 12-15, 2018, Beijing, China.
- **[CGO'18] CVR: Efficient SpMV Vectorization on X86 Processors.** **Biwei Xie**, Jianfeng Zhan, Zhen Jia, Wanling Gao, Lixin Zhang and Xu Liu. In Proceedings of the 2018 International Symposium on Code Generation and Optimization. Feb 24-28, 2018, Vienna, Austria.
- **[HPCC'16] Understanding Data Analytics Workloads on Intel Xeon Phi.** **Biwei Xie**, Xu Liu, Sally A McKee, Jianfeng Zhan, Zhen Jia, Lei Wang, and Lixin Zhang. In Proceedings of the 18th International Conference on High-Performance Computing and Communications. Dec 12-14, 2016, Sydney, Australia.
- **[IISWC'15] Characterizing Data Analytics Workloads on Intel Xeon Phi.** **Biwei Xie**, Xu Liu, Jianfeng Zhan, Zhen Jia, Yuqing Zhu, Lei Wang, and Lixin Zhang. In Proceedings of the 2015 IEEE International Symposium on Workload Characterization, short paper. Oct 4-6, 2015, Atlanta, USA.

Patents

- EP3104275A4. Data processing method, device and system. Lixin Zhang and **Biwei Xie**. Huawei Technologies Co., Ltd.

Professional Services

- Sponsorship Chair of Benchmarking, Measuring, and Optimizing (Bench), 2018.
- External Reviewer of Parallel Architectures and Compilation Techniques (PACT), 2018.
- Reviewer of Transactions on Parallel and Distributed Systems (TPDS), 2018.